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REMARKS

Claims 1-24 are pending in this application, of which Claims 1, 12, 23 and 24 are the independent claims. All claims stand rejected.

Claims 1-3, 5 and 23 are being amended to correct obvious drafting errors, replacing "multiplexer" and "multiplexing stage" with "demultiplexer." Claim 1 is also being amended to further clarify the scope of the claims, reciting "a lower frequency data demultiplexer coupled to the higher frequency demultiplexer." Claims 13-17 are being amended to correct obvious drafting errors, replacing "data communication circuit" with "method of demultiplexing."

Rejection of Claims 1-12 under 35 U.S.C. § 112

Claims 1-12 have been rejected for failing to particularly point out and distinctly claim the subject matter regarded as the invention. Claims 1-3 and 5 are being amended to correct obvious drafting errors. As a result of these amendments, it is believed that the § 112 rejection of claims 1-12 is no longer applicable, and reconsideration is respectfully requested.

Rejection of Claims 1-24 under 35 U.S.C. § 103

Claims 1-24 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Izadpanah (US Patent No. 6,240,274) in view of one or more of Lundh et al. (U.S. Patent No. 6,310,895), Kishigami et al. (U.S. Patent No. 5,787,132), Ishiwaka (U.S. Patent No. 6,310,913) and Chang (U.S. Patent No. 6,628,605). Applicants respectfully disagree and request reconsideration.

Claim 1 is directed to a data demultiplexer having a higher-frequency demultiplexer and a lower-frequency demultiplexor. An example data demultiplexer is illustrated in Fig. 14 and is not intended to limit the scope of the invention, being defined by the claims. Here, the data demultiplexor 103 includes a 1:2 input/output higher-frequency demultiplexor 190, followed by a 1:4 input/output lower-frequency demultiplexor. The data demultiplexor 103 receives a high-frequency data input signal 115 and a clock signal 117N/P. The higher-frequency demultiplexor 190 demultiplexes the data signal 115 into a 2-bit signal 203 having an intermediate frequency. This intermediate signal 203 is then received by a lower-frequency demultiplexor having latches

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199-202, which further demultiplexes the data signals to produce four 2-bit data signals 116 at a lower frequency.

Fig. 15 is a timing diagram illustrating signals at the data demultiplexer 103. The data input signal "in" 115 includes 8 multiplexed data segments a-h. The higher-frequency demultiplexer converts this input 115 to a 2-bit intermediate-frequency signal 203. Lastly, the lower-frequency demultiplexer converts this intermediate signal 203 to four 2-bit, lower-frequency data signals 116a-d. It can also be seen the clock signal bclk is precisely distributed to the higher-frequency demultiplexer 190, as the clock signal bclk has rising and falling edges that coincide with each segment of the data signal "in" 115. In contrast, the clock signal 190 is less precisely distributed to the lower-frequency demultiplexor, as the intermediate signal 203 only coincides with some of the rising and falling edges of the clock signal bclk.

Izadpanah discloses circuitry for wireless communication. The architecture of this circuitry is shown in Fig. 1, with a transmitting section 1 and a receiving section 2. At the transmitting section, a high bit-rate signal is received by a demultiplexer 7, where it is divided into several parallel sub-channels 9. Each of the sub-channels 9 is received by a modem 11. In order to transmit a respective sub-channel 9 over a wireless radio channel, each modem 11 applies the sub-channel 9 to a different carrier frequency provided by a radio-frequency oscillator 15 and harmonic generator 16. Thus, each modem 11 generates an analog signal 17 that carries a respective sub-channel 9 on a different frequency, which is then transmitted wirelessly at the antenna 23 to receiving circuitry 2.

Izadpanah fails to teach or suggest "further demultiplexing the intermediate frequency signal" as recited in Claim 1. In the Office Action, it is cited in Izadpanah that "Each individual modem of the bank of individual modems 11 is synchronized by a clock signal from a divider 14 which divides the frequency of the master clock 13 by N" (col. 3, lines 57-60). However, Izadpanah is merely stating that each modem 11 is clocked by a divided-down clock signal so that it is synchronized with a received sub-rate channel 9. Each modem 11 is not a "lower-frequency data demultiplexer" because it does not demultiplex the respective sub-rate channel 9. Rather, each modem 11 receives a single sub-rate channel 9, and outputs a single analog signal 17 that carries the data of the sub-rate channel 9 (col. 3, lines 53-57 and col. 4, lines 1-12). The modems 11 do not perform demultiplexing. Thus, Izadpanah discloses a single, high-frequency

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demultiplexer 7, but fails to disclose a lower-frequency demultiplexer to further demultiplex the output signals of the demultiplexer 7.

Lundh discloses a distribution of two different clocking signals, labeled "clock rate" and "synch rate" (col. 1, lines 15-19). When these two signals are distributed, they must be synchronized precisely so that the pulses of the "synch rate" align with the correct pulses of the "clock rate" (col. 1, lines 58-63). Lundh does not suggest a clock signal that is both "precisely distributed" to a higher frequency data demultiplexer and "less precisely" distributed to a lower frequency data demultiplexer, as now recited in Claim 1. Rather, Lundh simply states that two separate clock signals must be distributed precisely in order to remain synchronized. Moreover, Lundh, like Izadpanah, fails to disclose a higher frequency data demultiplexer and a lower frequency data demultiplexer. Thus, Lundh, alone or in combination with Izadpanah, fails to teach or suggest the invention as recited in Claim 1.

For at least the reasons stated above, Izadpanah and Lundh also do not teach the invention as recited in Claim 12. In particular, the cited references do not suggest "demultiplexing the data from the communication link to an intermediate frequency signal," and "further demultiplexing the intermediate frequency signal to a lower frequency signal." Claims 2-11 and 13-22 depend from one of Claims 1 and 12 and thus are allowable at least for the reasons stated above.

Given the shortcomings of Izadpanah and Lundh, one would find no assistance in Kishigami, Ishiwaka or Chang in discerning the present invention. None of the cited references disclose a data demultiplexer having higher and lower fequency data demultiplexers that are coupled by an intermediate frequency signal. As a result, the § 103 rejection of claims 1-24 is believed to be traversed, and reconsideration is respectfully requested.

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CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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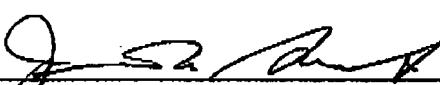
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